PCN ADG/21/13069

Catania, October 11th 2021

Automotive Discrete Group (ADG)
Power Transistor MACRO-Division
IGBT & IPM Business Unit

Process Change Notification

IGBT & IPM in Trench Field Stop Technology – Front end capacity Expansion to Samsung foundry

Dear Customer,

Following the continuous improvement of our service and in order to increase front-end capacity, this document is announcing the new 8" wafer line introduction at external foundry (Samsung – Korea) for IGBT Trench Field Stop Technology products listed in this PCN.
IGBT Trench Field Stop Technology manufactured in 8" wafer size at Samsung (Korea) foundry guarantees same quality and same electrical characteristics as per current production
The involved product series are listed in the table below:

Product Family	Technology	Test Vehicle type	Test vehicle Part numbers	Package	Implementation schedule
IGBT & IPM	IGBT Trench	Technology qualification (1 product in 3 package)	STGW40H65DFB	TO247	Wk02 2022
			STGWA40HP65FB	TO247 LL	Wk02 2022
			STGWT40HP65FB	TO3P	Wk02 2022
		Product qualification (1 test vehicle per package)	STGWA80H65DFB	TO247 LL	Wk16 2022
			STGW80H65DFB	TO247	Wk16 2022
			STGW80H65DFB-4	TO247-4L	Wk16 2022
			STGWT80H65DFB	TO3P	Wk16 2022
			STGB40H65FB	D2PAK	Wk16 2022
			STGFW40V60DF	TO3PF	Wk18 2022
			STGF20H60DF	TO220FP	Wk18 2022
			STGD5H60DF/DFSF	DPAK	Wk20 2022
			STGIB15CH60TS-L	SDIP2B-26L	Wk24 2022

Any other Product related to the above Product Family/Technology, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

Technology and product reliability test plan reports are provided in attachment to this document.

Samples availability:

Samples of the technology test vehicle devices will be available upon request. Any other sample request will be processed and scheduled by IGBT&IPM Business Unit, upon request.

Change implementation schedule:

The production start and first shipments will be implemented as per above table.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of devices affected by this process change will be ensured by internal code (Finished Good) and Q.A. number.

Yours faithfully.

IGBT Trench Gate FS Emitter Implant
Samsung Wafer Foundry Technology qualification

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Revision history

Rev.	Changes description	Author	Date
1.0	New release	M.Panzarella	September 20th , 2021

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	A. Marmoni	September 20th , 2021

Contents

1. Reliability Evaluation Overview

1.1. Objective and reliability strategy

Aim of this document is to present the qualification plan to be performed on a selected test vehicle to release in mass production the products designed in IGBT Trench Gate FS Emitter Implant Technology intended for standard application domain, diffused in Samsung Wafer Foundry.

The qualification activity will be performed on 3 diffusion lots assembled into 3 different packages:

Commercial product	Silicon line	Package	Assembly plant
STGW40H65DFB	EWF6	TO247	ST Shenzhen (China)
STGWA40HP65FB	EWF6	TO247-LL	TFME subcon (China)
STGWT40HP65FB	EWF6	TO3P	SPSEMI subcon (Korea)

The qualification plan is based on a full reliability stress test matrix according to **ST 0061692** specification for standard domain including Electrical Characterization and ESD Characterization.

Details of each stress test and relevant conditions are reported in the tables at section 1.2 and 2.

1.2. Test Plan

1.2.1. Test Plan Table

#	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	TEST	Pre- and Post- Stress Electrical Test	Yes
2	PC	Preconditioning	Not Applicable
3	EV	External Visual	Yes
4	PV	Parametric Verification	Yes
5	HTRB	High Temperature Reverse Bias	Yes
6	HTGB	High Temperature Gate Bias	Yes
7	TC	Temperature Cycling	Yes
8	AC	Autoclave	Yes
9	THB	Temperature Humidity Bias	Yes
10	IOL	Intermittent Operational Life	Yes
11	ESD	ESD Characterization	Yes

2. Test summary details

2.1. Test Summary table

Test method revision reference is the one active at the date of reliability trial execution.

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Comments
TEST	1		User specification or supplier's standard specification	3	241	723	All qualification parts
PC	2	-	-	-	-	-	Not applicable
EV	3	JESD22B-101I	All qualification parts submitted for testing	3	241	723	
PV	4	-	All parameters according to user specification at room, hot and cold temperature	3	25	75	
HTRB	5	MIL-STD-750-1 M1038 Method A	Tj=175°C, Vds=520V, 1000h	3	45	135	
HTGB	6 A	JESD22 A-108	Tj=175°C, Vgs= 20V, 1000h	3	45	135	
	6 B		Tj=175°C, Vgs= -20V, 1000h	3	45	135	
TC	7	JESD22A-104	Ta=-65°C /+150°C, 500cy	3	25	75	
AC	8	JESD22 A-102	Ta=121°C, Pa=2atm, RH=100%, 96h	3	25	75	
H3TRB	9	JESD22A-101	Ta=85°C, RH=85% Vds=100V, 1000h	3	25	75	
IOL	10	MIL-STD-750 Method 1037	10Kcy @ Ta=25°C with parts powered to ensure $\Delta Tj \geq 100°C$ (not to exceed absolute maximum ratings).	3	25	75	
ESD	11		HBM / CDM	1	6	6	3 for each configuration

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IGBT Trench Gate Emitter Implant
Samsung Wafer Foundry
Product transfer

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Revision history

Rev.	Changes description	Author	Date
1.0	New release	M.Panzarella	September 20th , 2021

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	A. Marmoni	September 20th , 2021

Contents

1. Reliability Evaluation Overview

1.1. Objective and reliability strategy

In order to release Samsung wafer Foundry as third source for product manufacturing design in IGBT Trench Gate FS Emitter Implant Technology intended for standard application domain, a qualification is now running by means a selected test vehicle assembled in 3 different packages:

Commercial product	Silicon line	Package	Assembly plant
STGW40H65DFB	EWF6	TO247	ST Shenzhen (China)
STGWA40HP65FB	EWF6	TO247-LL	TFME subcon (China)
STGWT40HP65FB	EWF6	TO3P	SPSEMI subcon (Korea)

Aim of this qualification plan is to present the reliability evaluation to be performed on selected test vehicles chosen as worst case based on maximum die size for all the other involved packages, see below the list matrix:

Commercial product	Silicon line	Package	Assembly plant
STGWA80H65DFB	EWFR	TO247 LL	TFME subcon (China)
STGB40H65FB	EWF6	D2PAK	ST Shenzhen (China)
STGW80H65DFB	EWFR	TO247	ST Shenzhen (China)
STGW80H65DFB-4	EWFR	TO247-4L	TFME subcon (China)
STGWT80H65DFB	EWFR	TO3P	SPSEMI subcon (Korea)
STGFW40V60DF	EVF6	TO3PF	SPSEMI subcon (Korea)
STGF20H60DF	EIFE	TO220FP	ST Shenzhen (China)
STGD5H60DF	EI62	DPAK	ST Shenzhen (China)
STGD5H60DFSF	EI62	DPAK	TFME subcon (China)

The qualification purpose will be addressed to verify the failure mode related to the Front-End (Silicon Technology) vs Back-End (Package Typology) interactions applying the path described here below:

1.2. Test Plan

1.2.1. Test Plan Table

#	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	TEST	Pre- and Post- Stress Electrical Test	Yes
2	PC	Preconditioning	Yes
3	EV	External Visual	Yes
4	PV	Parametric Verification	Yes
5	HTRB	High Temperature Reverse Bias	Similarity (generic data)
6	HTGB	High Temperature Gate Bias	Similarity (generic data)
7	TC	Temperature Cycling	Yes
8	AC	Autoclave	Yes
9	THB	Temperature Humidity Bias	Yes
10	IOL	Intermittent Operational Life	Yes
11	ESD	ESD Characterization	Yes

2. Test summary details

2.1. Test Summary table

Test method revision reference is the one active at the date of reliability trial execution.

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Comments
TEST	1		User specification or supplier's standard specification	1	106	106	All qualification parts
PC	2	JESD020E	24h bake@125°C MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 245°C or 260°C	1	100	100	All devices to be subjected to H3TRB, TC, AC and IOL Performed on 1 lot per each product mentioned in the table at pag3 of this report (If SMD package)
EV	3	JESD22B-101I	All qualification parts submitted for testing	1	106	106	Performed on 1 lot per each product mentioned in the table at pag3 of this report
PV	4	User Specification	All parameters according to user specification at room, hot and cold temperature	1	25	25	Performed on 1 lot per each product mentioned in the table at pag3 of this report
HTRB	5	MIL-STD-750-1 M1038 Method A	-	-	-	-	Family data
HTGB	6	JESD22 A-108	-	-	-	-	Family data
TC	7	JESD22A-104	Ta=-65°C /+150°C, 500cy	1	25	25	Performed on 1 lot per each product mentioned in the table at pag3 of this report
AC	8	JESD22 A-102	Ta=121°C, Pa=2atm, RH=100%, 96h	1	25	25	Performed on 1 lot per each product mentioned in the table at pag3 of this report
H3TRB	9	JESD22A-101	Ta=85°C, RH=85% Vds=100V, 1000h	1	25	25	Performed on 1 lot per each product mentioned in the table at pag3 of this report
IOL	10	MIL-STD-750 Method 1037	10Kcy @ Ta=25°C with parts powered to ensure $\Delta Tj \geq 100°C$ (not to exceed absolute maximum ratings).	1	25	25	Performed on 1 lot per each product mentioned in the table at pag3 of this report
ESD	11	JEDEC JS-001 & JS-002	HBM / CDM	1	6	6	Performed on 1 lot per each product mentioned in the table at pag3 of this report

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STGIB15CH60TS-L (RI64P1) / SDIP2B-26L
Intelligent Power Module
Samsung Wafer Foundry Product transfer

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Revision history

Rev.	Changes description	Author	Date
1.0		G. Carra'	07th October 2021

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	A. Marmoni	07th October 2021

Contents

1. Reliability Evaluation Overview

1.1. Objective and reliability strategy

In order to release Samsung wafer Foundry as third source for product manufacturing design in IGBT Trench Gate FS Emitter Implant Technology intended for standard application domain, a qualification plan is running on following vehicles:

Commercial product	Silicon line	Package	Assembly plant
STGW40H65DFB	EWF6	TO247	ST Shenzhen (China)
STGWA40HP65FB	EWF6	TO247-LL	TFME subcon (China)
STGWT40HP65FB	EWF6	TO3P	SPSEMI subcon (Korea)

Aim of this document is to present the qualification plan to release in mass production the Intelligent Power Module **STGIB15CH60TS-L** (RI64P1 as ST internal line) intended for Industrial application designed in IGBT Field Emitter Implant Trench MOSFET Technology, diffused in Samsung Foundry Wafer Fab and assembled in package SDIP2B-26L in ST Shenzhen (China) assembly plant.
The reliability evaluation will be performed according to **ST 0061692** specification.

Details of each stress test and relevant conditions are reported on section 2 table.

1.2. Test Plan

Test Plan Table

#	TEST NAME	TEST FLAG
1	Pre and Post Stress Electrical Test	Yes
2	External Visual	Yes
3	Preconditioning (PC)	No
4	Thermal Cycling (TC)	Yes
5	Vibration (V)	No
6	(Intermittent Operational Life/Thermal Fatigue) IOL/TF (PCmin)	Yes
7	PCsec (Pwcy)	No
8	AutoClave (AC)	Yes
9	High Temperature Storage (HTS)	No
10	Low Temperature Storage (LST)	No
11	High Temperature Reverse Bias (HTRB)	No
12	High Temperature Gate Bias (HTGB)	No
13	Temperature Humidity Bias (THB)	Yes

2. Test summary details

2.1. Test Summary table

Test method revision reference is the one active at the date of reliability trial execution.

Test #	Reference	Test name	STM Test Conditions	Lots	S.S.	Total	Comments
1		Pre and Post Stress Electrical Test	According to user specification or supplier's standard specification	1	30	30	All qualification parts before/after stress
2		External Visual		1	30	30	All qualification parts before/after stress
3	According to JESD22-A113 JSTD-020	Preconditioning	24h bake @125°C Store 168H @ TA=85°C RH=85% 3x IR Reflow @ 260°C	-	-	-	All qualification parts
4	According to JESD22 A-104	Thermal Cycling (TC)	Ta= -40°C/125°C, duration= 1000cy	1	6	6	
5		Vibration (V)		-	-	-	
6	MIL-STD-750 Method 1037	IOL/TF (PCmin)	ΔTj≥100°C, **cycles≥6K** cycle duration =2min	1	6	6	
7	MIL-STD-750 Method 1037	PCsec	ΔTj≥100°C, **cycles≥15K** cycle duration =7s	-	-	-	
8	According to JESD22 A-102	AutoClave	TA=121°C; PA=2ATM	1	6	6	
9	According to JESD22 A-103	High Temperature Storage (**HTS**)	Ta=150°C, duration=1000h	-	-	-	
10	According to JESD22 A-103	Low Temperature Storage (**LTS**)	Ta=-40°C, duration=1000h	-	-	-	
11	According to JESD22 A-108	High Temperature Reverse Bias (**HTRB**)	Vbias=0.8 Vdd, Ta=150°C, duration=1000h	-	-	-	
12	According to JESD22 A-108	High Temperature Gate Bias (**HTGB**)	Vbias=Vgs max, Ta=150°C, duration=1000h	-	-	-	
13	According to JESD22 A-101	Temperature Humidity Bias (**THB**)	Vbias=80V, Ta=85°C, RH=85%, duration=1000h	1	6	6	

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